

AN ERROR DETECTOR AND AUTOMATIC CONTROL
UNIT DESIGNED FOR USE WITH THE
LINE SPEED BUFFER

I. INTRODUCTION

An error detector and automatic control unit was designed to eliminate errors caused during transmission of a message from one line-speed buffer⁽¹⁾ to another. The line-speed buffer is a magnetic tape device which accepts information at keyboard speeds and is capable, at some later time, to transfer the information to a distant buffer at a much higher information rate. A dial-up telephone line is used as the transmission medium between transmitting and receiving buffers. After receiving the information, the receiving buffer can be operated at a slower speed to reduce the information rate so that a printer can accept and print the received information.

The error detector and automatic control unit is designed to function with the line-speed buffer while transmitting information over dial-up telephone lines and while using the AT & T Model 202A or Model 3A subsets. Detection of errors is accomplished by information block parity comparison. The message to be transmitted is prepared on a magnetic tape in blocks of approximately 150 characters and with spaces, of noise-free tape, equivalent to ten characters between blocks. Each block of information is coded into ten parity bits which are compared after the transmission of each information block. If the parity bits coded at the transmitter from the transmitted block of information compare

with the parity bits coded at the receiver from the received block of information, the information was correctly received and the automatic control unit will instruct the transmitter to transmit the next block of information. If the parity coded from the transmitted information does not compare with the parity coded from the received information, the information block is taken as being received incorrectly. Correction of erroneous information blocks is accomplished by retransmission of the information block found to be in error.

The automatic control unit contains sufficient logic to control the line-speed buffer in performing such functions as tape start, tape forward, tape back, and tape stop. The logic decisions are influenced by both present and past history of operation. The control sequence of the line-speed buffer by the automatic control unit can be divided into five fairly well defined steps. These five control steps are referred to as CS_1 (Control Step No. 1) through CS_5 . During CS_1 a signal is sent to the data phone as a notification that a block of information is to be transmitted. CS_2 is the period during which 2 blocks of information is transferred from one buffer to another. CS_3 is a period set aside for the parity generated at the transmitter to be sent to the receiver and compared with the parity generated at the receiver. During CS_4 an acknowledgement signal indicating whether the parity check was correct or incorrect is sent from the receiver to the transmitter. If the parity bits are not identical, CS_5 is the period during which both transmitter and

receiver buffer tapes are reversed to prepare for the retransmission of the incorrectly received block of information. The control sequence goes from CS₅ to CS₁ and repeats the same sequence. If the parity bits are identical, CS₅ is not actuated; and the control sequence goes from CS₄ directly to CS₁ and continues the process.

II. LINE-SPEED BUFFER

The line-speed buffer is a magnetic tape device whose principal feature, among other desirable ones, is to record information at keyboard speeds and to transfer this recorded information to another buffer at the maximum information rates permitted by dial-up telephone lines. The line-speed buffer was designed to accept parallel information from a keyboard such as the teletype model 28 and to record the information on magnetic tape in serial-by-bit form. The parallel to serial conversion is accomplished with the recording head. During the recording of information from the keyboard to the magnetic tape, the line-speed buffer advances the magnetic tape in incremental steps to provide equal spacing of the characters on the tape. The characters are recorded on the magnetic tape in the normal "start plus five-bit teletype code" and are recorded at a character density of ten characters per inch of tape.

During transmission of the prepared message to the receiving line-speed buffer, the receiving as well as the transmitting buffer is operating at a tape speed of approximately 16 ips (inches per second). When operating over dial-up telephone lines and with the AT & T Model 202A subsets, the line-speed buffer utilizes the telephone equipment to the utmost by transmitting the message at a rate of 160 characters per second, or in more general terms, approximately 1600 words per minute. The transmission of information between buffers is accomplished in serial-by-bit form and in the NRZI (transition) code. An

NRZI converter, at the transmitting buffer, is used to change the pulse output from the tape to binary information containing a transition corresponding to a one and a transition (either positive or negative going) in the information from the NRZI converter also corresponds to a one.

Once the information has been recorded at the receiving buffer, the receiving buffer can be operated at a continuous speed of one inch per second to print the received information on a unit such as the Teletype Model 28 printer. For additional information concerning the line-speed buffer, consult reference 1.

III. DATA PHONE

The AT & T Model 3A and Model 202A Data Phones operate in identical fashion. The Model 202A is the later model and is more compact than the Model 3A. Both models are capable of transmitting up to 1200 bits of information over dial-up telephone lines. Only Model 202A shall be referred to during the following discussion.

The AT & T Model 202A Data phone is a digital subset manufactured by the American Telephone and Telegraph Company. A brief description of the data phone and its function in transmitting information over dial-up telephone lines between two line-speed buffers will be an aid in understanding the operation of the automatic control unit.

The data phones are physically placed in the total system as illustrated in Figure 1. The telephone is actually an integral part of the Model 202A Data phone, but in Figure 1 the telephone is shown as a separate unit to clarify its function in the system. The description to be presented will be for data phones which are wired to operate over telephone lines utilizing echo suppressors. The primary functions of the data phones are to modulate (modify the binary data so that it is easily transmitted over the telephone line) the binary data sent at the transmitting buffer and to demodulate (recover the binary data from the received modulated signal) the received information at the receiving buffer.

A telephone line connection must be obtained between the data-phone located at the two line-speed buffers before information can be

transmitted from one buffer to the other. This connection is easily obtained by the operator of the buffer to be used for transmitting data. The operator simply picks up the telephone receiver located on the data phone; and when a dial tone is heard, dials the telephone number of the data phone for the intended receiver. The attendant at the receiving buffer answers the telephone, and through voice communication with the operator of the transmitting buffer, can state when the receiver is ready to accept the message to be transmitted. Once the transmitting buffer is ready to send a message and the intended receiver is prepared to accept the message, the data button on the data phones can be depressed and the telephone receivers can be placed in their normal position. The data buttons are depressed to connect the data phones to the telephone line.

As shown in Figure 1, the error detector and automatic control unit is connected to the data phone through five information lines in addition to a common ground. All signals sent to the data phone from the Error Detector and Automatic Control Unit must have a minimum amplitude of -3 to +3 volts and a maximum amplitude no greater than -20 to +20 volts. All signals sent from the data phone to the error detector and automatic control unit have an approximate amplitude of -8 to +8 volts.

Preceding the transmission of a block of data, a positive potential (potential above ground) must be applied to the request - send line. The data phone, when receiving this signal, places a carrier signal on the tele-

phone line between the two data phones. The carrier-on-off signal becomes approximately +9 volts when the carrier signal is detected at the receiving data phone. A time delay will be experienced between the injection of a carrier signal at the transmitter and the carrier-on-off signal going positive at the receiver. The delay is a function of the amplitude response as well as the time delay of the telephone line. Therefore, the delay will generally be longer for telephone lines of long distances than for lines of short distances. The carrier-on-off signal will be negative in potential when no carrier is present on the telephone line.

The clear-to-send signal at the data phone which had provided the request-send signal will become a positive 8 volts approximately 200 ms after a positive signal had been placed on the request-send line. A positive clear-to-send signal indicates that the dataphone is ready to accept binary data which is to be transmitted over the telephone line. The 200 ms delay between the clear-to-send signal going positive and the request send signal going positive is strictly a function of the data phone. This time duration is provided to allow the telephone line sufficient time to be turned around. In other words, to allow sufficient time for establishing the carrier signal on the telephone line and in the proper direction (from the transmitting data phone to the receiving data phone).

IV. ERROR DETECTOR

The detection of errors in the received information is accomplished by block parity check. The information to be transmitted is prepared in blocks of approximately 150 characters with a space equivalent to ten characters of noise-free tape between blocks. Each character is coded in the normal teletype code (start plus five information bits). The automatic control unit contains a start-stop clock which starts approximately a half-bit time after the start bit is introduced to the unit from the line-speed buffer and operates for six clock periods before being stopped by a counter. The first of these six clock pulses is used to change the state of a binary flip-flop which throughout this paper shall be referred to as the sampling flip-flop. The remaining five clock pulses are used to trigger the sampling flip-flop which samples the five information bits of each character. This sampling process at the transmitting buffer is performed primarily to eliminate jitter in the data caused by speed variations of the line-speed buffer. These speed variations are very small and the sampling process could probably be eliminated at the transmitting buffer; but since the sampling flip-flop is definitely needed when the buffer is used as a receiver, the slight jitter in the data can be removed with no addition to the necessary electronic circuits.

As mentioned above, the last five of six clock pulses are used to drive the sampling flip-flop. Groups of these five clock pulses will be referred to as Cl_3 . The positive going transitions of Cl_3 are delayed

approximately 100 microseconds to form the pulses of Cl_4 which is used to drive the error-detector register. The information encoded by the error-detector register is taken from the sampling flip-flop. In order to encode the five information bits of each character instead of the start and the following four information bits, the clock driving the error-detector register must be delayed from the clock driving the sampling flip-flop. The delay of Cl_4 beyond Cl_3 also plays an important role during the parity check at the receiver. This will be explained in greater detail during the discussion of parity comparison. Refer to Figure 2 for a timing relation between Cl_1 , Cl_2 , Cl_3 , Cl_4 , information sent to the sampling flip-flop, and information sent from the sampling flip-flop.

The error detector register, shown in Figure 3, consists of ten flip-flops and one Exclusive OR gate. The equation of the sequence generated by the error-detector register is

$$X^{10} + X^9 + 1 = 0,$$

where + represents Exclusive OR. This expression may be stated that the feedback (X^{10}) is equal to the sum, mod-2, of the first flip-flop (X^0) on the right and the tenth flip-flop (X^9) from the right. Flip-flop (X^9) is connected such that its output at time $(t_1 + 1)$ is equal to the sum, mod-2 of its contents at time t_1 and the output of the Exclusive OR gate at time t_1 . This connection of flip-flop (X^9) eliminates the need of one Exclusive OR gate. The Exclusive OR gate included in the error-detector register sums, mod 2, the output of flip-flop (X^0) and the data input from the

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sampling flip-flop. By this method, the data has an influence on the sequence generated in the ten-stage register. The sampling flip-flop, after reclocking the information from the transmitting buffer, sends the information to the error-detector register for encoding and to the data phone for transmission of the information to the receiving buffer. The encoding and transmitting processes take place simultaneously. After a block of information has been transmitted and encoded, the ten bits remaining in the ten-stage register comprise the parity for the block of information transmitted.

At the receiver, the identical encoding process takes place. The incoming information from the data phone is sampled by the sampling flip-flop and its output is sent to the error-detector register. If the information block is received correctly, the ten bits, remaining in the ten-stage register after the information block has been received, will compare exactly to the ten bits remaining in the ten-stage register at the transmitter after the block of information has been transmitted.

The ten parity bits generated at the transmitter are sampled and a start bit is added to each group of five parity bits by the sampling flip-flop before the parity is transmitted to the receiver. The advantage of dividing the parity into two groups of five bits plus a start bit is that the parity is molded into a form identical to the information characters. This allows the parity to be processed by the identical clocks that are used to process the information characters. The added start bit is

required to actuate the start-stop clock.

The ten parity bits generated at the transmitter are transmitted to the receiver approximately ten milliseconds after the information block had been transmitted. In other words, the parity for a block of information is separated from the block with a gap equivalent to ten milliseconds. This gap between the information block and its parity is entered at the transmitter so that the automatic control unit at the receiver can determine where the information block ends and where the parity begins. The parity received from the transmitter is compared with the parity generated at the receiver in the Exclusive OR gate which is a part of the error-detector register (Figure 3) at the receiver. The output of the Exclusive OR gate is sampled at appropriate times to determine whether the parity check was correct or incorrect. Parity comparison shall be discussed in greater detail in the section devoted to the automatic control unit.

This scheme of error detection can detect $1 - \frac{1}{2^{10}}$ of all possible errors occurring in each information block. In other words, the number of undetected errors will amount to a fraction $\frac{1}{2^{10}}$ of all possible errors. Therefore, the error detection is approximately 99.9% effective. The efficiency of the error detection scheme can be increased by increasing the number of flip-flops in the error detection register which will amount to an increase in the number of parity bits for each block of information.